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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/692,543	10/24/2003	Michael Frisch	21334-1264	1110
29450	7590	01/13/2005	EXAMINER	
BARLEY SNYDER, LLC 1000 WESTLAKES DRIVE, SUITE 275 BERWYN, PA 19312			WILLIAMS, ALEXANDER O	
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 01/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>		<b>Applicant(s)</b>	
	10/692,543		FRISCH ET AL.	
	<b>Examiner</b>		<b>Art Unit</b>	
	Alexander O Williams		2826	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

**A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.**

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 29 September 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-38 is/are pending in the application.
- 4a) Of the above claim(s) 3,7-11,13-16 and 26-38 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,4-6,12 and 17-25 is/are rejected.
- 7) ☒ Claim(s) 2 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)               | Paper No(s)/Mail Date. _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>6/9 &amp; 4/9/04</u>  | 6) <input checked="" type="checkbox"/> Other: <u>IDS 10/24/03</u>           |

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Serial Number: 10/692543 Attorney's Docket #: 21334-1264

Filing Date: 10/24/2003; claimed foreign priority to 10/30/02

Applicant: Frisch et al.

Examiner: Alexander Williams

Applicant's election of the species of II, figure 2 (claims 1, 2, 4-6, 12 and 17-25), filed 9/29/04, has been acknowledged.

This application contains claims 3, 7-11, 13-16 and 26-38 drawn to an invention non-elected without traverse.

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The disclosure is objected to because of the following informalities: On page 17, lines 10-11, states "Fig. 2 shows an embodiment wherein the substrate 110 is connected to the latent heat storage module 104" and on line 15, number 106, Fig. 2 DO NOT show theses numbers labeling the items. On page 15, line 11, should "ceramics" be -ceramic--?

Appropriate correction is required.

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The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the claim language of claims 19, 21 and 22 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claims 19, 21 and 23 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

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In claim 19, it is unclear and confusing to how the claim language of "wherein the semiconductor component is connected to the substrate by a press-fit connection" reads on the elected species of figure 2. What features describes this?

In claim 21, it is unclear and confusing to how the claim language of "wherein the semiconductor component is electrically connected on an upper side thereof by at least one wire bonded connection" reads on the elected species of figure 2. What features describes this?

In claim 23, it is unclear and confusing to how the claim language of "wherein the semiconductor component is electrically connected on an upper side thereof by at least one press-fit connection" reads on the elected species of figure 2. What features describes this?

Any of claims 19, 21 and 23 not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

Patentability shall not be negated by the manner in which the invention was made.

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This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 4-6, 12, 17-19 and 21-25, **insofar as claims 19, 21 and 23 can be understood**, are rejected under 35 U.S.C. § 102(b) as being anticipated by Ishikawa (Japan Patent # 4-101450).

1. Ishikawa (figures 1-5) specifically figure 1 show an integrated circuit system **11** comprising: at least one integrated circuit having a substrate (inherit within A) with at least one semiconductor component **A** assembled on the substrate;  
a cooling body **10** configured to dissipate heat generated by the integrated circuit; and  
a latent heat storage module **14,15,16** having a latent heat storage medium which is thermally connected to the cooling body to temporarily store the heat generated by the integrated circuit and to convey it to the cooling body, the substrate being in direct thermal contact with the latent heat storage module.
4. An integrated circuit system according to claim 1, Ishikawa show wherein the substrate is mechanically fixed to the latent heat storage module by a material-joining connection (inherit).
5. An integrated circuit system according to claim 4, Ishikawa show wherein the material-joining connection is formed by soldering, welding or gluing (inherit).
6. An integrated circuit system according to claim 1, Ishikawa show wherein the latent heat storage module has a latent heat storage housing which forms a hollow body filled with the latent heat storage medium.
12. An integrated circuit system according to claim 1, Ishikawa show wherein the latent heat storage housing includes a wall in thermal contact with the cooling body and at least partially formed by the cooling body.
17. An integrated circuit system according to claim 1, Ishikawa show wherein the semiconductor component is connected to the substrate by a soldered connection (inherit).

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18. An integrated circuit system according to claim 1, Ishikawa show wherein the semiconductor component is connected to the substrate by a glued connection (inherit).
22. An integrated circuit system according to claim 1, Ishikawa show wherein the semiconductor component is electrically connected on an upper side thereof by at least one joined connection.
24. An integrated circuit system according to claim 1, Ishikawa show wherein the cooling body has at least one cooling rib **26** for conveyance of heat (see figure 4).
25. An integrated circuit system according to claim 1, Ishikawa show wherein the cooling body is connectable to a cooling circuit (inherit).

Claim 20 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Ishikawa (Japan Patent # 4-101450) in view of Kawamoto et al. (Japan Patent # 59-35786).

Ishikawa show the features of the claimed invention as detailed above, but fail to explicitly show wherein the latent heat storage medium is paraffin.

Kawamoto et al. is cited for showing a latent heat storage body. Specifically, Kawamoto et al. (figures 1) discloses a latent heat storage medium **2** having a paraffin wax is used for the purpose of increasing the heat radiation velocity of the latent heat storage body.

Therefore, it would have been obvious to one of ordinary skill in the art to use Kawamoto et al.'s teaching of a paraffin wax used with the latent heat storage medium to modify Ishikawa's latent heat storage medium for the purpose of increasing the heat radiation velocity of the latent heat storage body.

Claims 1, 4-6, 12, 17-19 and 21-25, **insofar as claims 19, 21 and 23 can be understood**, are rejected under 35 U.S.C. § 103(a) as being unpatentable over Ellsworth, Jr. et al. (U.S. Patent Application Publication # 2003/0203181 A1) in view of Ishikawa (Japan Patent # 4-101450).

1. Ellsworth, Jr. et al. (figures 1a to 3) specifically figures 2 show an integrated circuit system **10** comprising: at least one integrated circuit **12** having a substrate with at least one semiconductor component **14** assembled on the substrate **16**; a cooling body **20** configured to dissipate heat generated by the integrated circuit; and a latent heat storage module (a structured cell/laminate may be employed as a thermal energy storage unit which can provide thermal load-

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damping capabilities due to its latent heat effect ) having a latent heat storage medium which is thermally connected to the cooling body to temporarily store the heat generated by the integrated circuit and to convey it to the cooling body, but fail to explicitly show the substrate being in direct thermal contact with the latent heat storage module. However, Ellsworth, Jr. et al. does disclose a semiconductor chip directly in thermal contact with the energy storage unit.

DOCUMENT-IDENTIFIER: US 20030203181 A1

TITLE: Interstitial material with enhanced thermal conductance for semiconductor device packaging

Abstract Paragraph - ABTX (1):

A thermal interface material for conducting thermal energy between a first surface and a second surface is disclosed. In an exemplary embodiment, the thermal interface material includes a non-metallic support layer and a phase change material coated on the support layer. At a transition temperature of the phase change material, the phase change material is caused to flow into gaps present between the support layer and the first and second surfaces. In addition, phase change compound (PCC) materials may be formulated to solid phase transition over a desired temperature range, such that in a the solid phase transition mode, a structured cell/laminate may be employed as a thermal energy storage unit which can provide thermal load-damping capabilities due to its latent heat effect.

Ishikawa is cited for showing a cooling apparatus. Specifically, Ishikawa (figures 1-5) specifically figure 1 discloses having a latent heat storage medium **15,14** which is thermally connected to the cooling body **10** to temporarily store the heat generated by the integrated circuit **A** and to convey it to the cooling body, the substrate (inherent within **A**) being in direct thermal contact with the latent heat storage module for the purpose of reducing the size and weight of a radiator fan by storing the heat produced by a semiconductor device or the like induced by short circuit during super heat as a latent heat and absorbing the heat.

4. An integrated circuit system according to claim 1, the combination with Ellsworth, Jr. et al. showing wherein the substrate is mechanically fixed to the latent heat storage module by a material-joining connection (the chip 14 is bonded to the module).



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5. An integrated circuit system according to claim 4, the combination with Ellsworth, Jr. et al. showing wherein the material-joining connection is formed by soldering, welding or gluing (the chip 14 is bonded to the module).
6. An integrated circuit system according to claim 1, the combination with Ellsworth, Jr. et al. showing wherein the latent heat storage module has a latent heat storage housing which forms a hollow body filled with the latent heat storage medium.
11. An integrated circuit system according to claim 10, the combination with Ellsworth, Jr. et al. showing wherein two or more semiconductor components **14** are provided having different bulk potentials, and various thermal coupling elements electrically insulated from one another are provided for the semiconductor components with different bulk potentials.
12. An integrated circuit system according to claim 1, the combination with Ellsworth, Jr. et al. showing wherein the latent heat storage housing includes a wall in thermal contact with the cooling body and at least partially formed by the cooling body.
17. An integrated circuit system according to claim 1, the combination with Ellsworth, Jr. et al. showing wherein the semiconductor component is connected to the substrate by a soldered connection (the chip 14 is bonded to the module).
18. An integrated circuit system according to claim 1, the combination with Ellsworth, Jr. et al. showing wherein the semiconductor component is connected to the substrate by a glued connection (the chip 14 is bonded to the module).
22. An integrated circuit system according to claim 1, the combination with Ellsworth, Jr. et al. showing wherein the semiconductor component is electrically connected on an upper side thereof by at least one joined connection.
24. An integrated circuit system according to claim 1, the combination with Ellsworth, Jr. et al. showing wherein the cooling body has at least one cooling rib for conveyance of heat.
25. An integrated circuit system according to claim 1, the combination with Ellsworth, Jr. et al. showing wherein the cooling body is connectable to a cooling circuit.

Therefore, it would have been obvious to one of ordinary skill in the art to use Ishikawa's substrate being in direct thermal contact with the latent heat storage module to modify Ellsworth, Jr. et al.'s semiconductor chip directly in thermal contact with the energy storage unit for the purpose of reducing the size and weight of a radiator fan by storing the heat produced by a semiconductor device or the like induced by short circuit during super heat as a latent heat and absorbing the heat.

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Claim 20 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Ellsworth, Jr. et al. (U.S. Patent Application Publication # 2003/0203181 A1) in view of Ishikawa (Japan Patent # 4-101450) and further in view of Kawamoto et al. (Japan Patent # 59-35786).

The Ellsworth, Jr, et al./Ishikawa combination show the features of the claimed invention as detailed above, but fail to explicitly show wherein the latent heat storage medium is paraffin.

Kawamoto et al. Is cited for showing a latent heat storage body. Specifically, Kawamoto et al. (figures 1) discloses a latent heat storage medium 2 having a paraffin wax is used for the purpose of increasing the heat radiation velocity of the latent heat storage body.

Therefore, it would have been obvious to one of ordinary skill in the art to use Kawamoto et al.'s teaching of a paraffin wax used with the latent heat storage medium to modify Ishikawa/Ellsworth Jr. et al.'s combination of a latent heat storage medium for the purpose of increasing the heat radiation velocity of the latent heat storage body.

Claim 2 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.. Any such indication as to the allowability of these claims is reserved until which time a suitable response is filed.

The listed references are cited as of interest to this application, but not applied at this time.

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Field of Search	Date
U.S. Class and subclass: 257/712,717,713,714,715,716,720,721,722,723.728,724, 725,729,731,E23.089 428/307.3,913,319.1,319.3 165/10,80.3 62/3.2,259.2,3.7,185,435,434,439,129,59,181	1/9/05
Other Documentation: foreign patents and literature in 257/712,717,713,714,715,716,720,721,722,723.728,724, 725,729,731,E23.089 428/307.3,913,319.1,319.3 165/10,80.3 62/3.2,259.2,3.7,185,435,434,439,129,59,181	1/9/05
Electronic data base(s): U.S. Patents	1/9/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'Alexander O Williams', is positioned above the printed name.

Alexander O Williams  
Primary Examiner  
Art Unit 2826

AOW  
1/10/05